CLAIMS

What is claimed is:

1. A direct memory access (DMA) system for transferring information between a master device (30) and a slave device (40) comprising: a first plurality of DMA channels for transferring information from said master device (30) to said slave device (40); a second plurality of DMA channels for transferring information from said slave device (40) to said master device (30); a first set of control registers (Figs. 6a, 6c, 6d, 6e, 6h, 6i, 6j) which coordinate use of said first plurality of DMA channels to transfer information from said master device (30) to said slave device (40); and a second set of control registers (Figs. 6b, 6c, 6f, 6g, 6h, 6k, 6l) which coordinate use of said second plurality of DMA channels to transfer information from said slave device (40) to said master device (30), wherein both said first set of control registers and said second set of control registers include at least one mailbox register (Figs. 6d, 6f) for selectively providing an interrupt signal to a respective one of said master device (30) and said slave device (40), in response to data written to said at least one mailbox register by the other of said master device and said slave device, during said DMA transaction.

2. The system of claim 1, wherein each of said first and second sets of control registers further comprise a mailbox interrupt status/control register (Figs. 6a,6b) for enabling/disabling mailbox interrupt generation for each of said at least one mailbox registers and for indicating whether one of said at least one mailbox interrupts is pending for each of said at least one mailbox registers.

3. The system of claim 1, wherein each of said first and second sets of control registers further comprise at least one scratch register (Figs. 6e,6g) for storing data which can be read in response to said interrupt signal generated by said at least one mailbox register.

4. The system of claim 1, further comprising a DMA interrupt status/control register (Fig. 6h) for enabling/disabling data transfer complete interrupt generation associated with a completion of transferring said information and for indicating whether one of said data transfer complete interrupts is pending for each of said first and second DMA channels.

5. The system of claim 1 further comprising: a first address register for storing a first address associated with one of said first plurality of DMA channels; a second address register for storing a second address associated with another of said first plurality of DMA

channels; a third address register for storing a third address associated with one of said second plurality of DMA channels; and a fourth address register for storing a fourth address associated with another of said second plurality of DMA channels.

6. The system of claim 1, further comprising: a first size register for storing a size of said information transferred using one of said first plurality of DMA channels; a second size register for storing a size of said information transferred using another of said first plurality of DMA channels; a third size register for storing a size of said information transferred using one of said second plurality of DMA channels; and a fourth size register for storing a size of said information transferred using another of said first plurality of DMA channels.

7. The system of claim 1, further comprising: a DMA status/control register (Fig. 6c) for indicating, for each of said first and second plurality of DMA channels, whether DMA transfer activity is ongoing.

8. The system of claim 1, wherein said data written to said at least one mailbox register is a command requesting that more data be transferred.

9. The system of claim 1, wherein said data written to said at least one mailbox register is a command to activate a feature of one of said slave device and said master device.

10. The system of claim 9, wherein said feature is a reduce power consumption feature.

11. A method for direct memory access (DMA) information transfer between a master device (30) and a slave device (40) comprising the steps of: storing a first data portion received during a DMA transaction using a first DMA channel; storing a second data portion received during said DMA transaction using a second DMA channel; and selectively providing an interrupt signal to one of said master device (30) and said slave device (40), by writing data in at least one mailbox register (Figs. 6d, 6f) by the other of said master device (30) and said slave device(40), during said DMA transaction.

12. The method of claim 11, further comprising the step of: enabling/disabling mailbox interrupt generation for each of said at least one mailbox registers (Figs. 6d,6f) and for indicating whether one of said at least one mailbox interrupts is pending for each of said at least one mailbox registers using a mailbox interrupt status/control register (Figs. 6a, 6b).

13. The method system of claim 11, further comprising the step of: reading data stored in at least one scratch register (Figs. 6e, 6g) in response to said interrupt signal.

14. The method of claim 11, further comprising the step of: enabling/disabling data transfer complete interrupt generation associated with a completion of storing said first and second data portions and for indicating whether one of said data transfer complete interrupts is pending for each of said first and second DMA channels using a DMA interrupt status/control register (Fig. 6h).

15. The method of claim 11 further comprising the steps of: storing a first address associated with said first DMA channel; and storing a second address associated with said second DMA channel.

16. The method of claim 11, further comprising the steps of: storing a size of said first data portion; and storing a size of said second data portion.

17. The method of claim 11, further comprising the step of: providing an indication regarding whether transfer activity is currently ongoing in said first and second DMA channels.

18. The method of claim 11, wherein said data written to said at least one mailbox register is a command requesting that more data be transferred.

19. The method of claim 11, wherein said data written to said at least one mailbox register is a command to activate a feature of one of said slave device and said master device.

20. The method of claim 19, wherein said feature is a reduce power consumption feature.

21. The method of claim 15, further comprising the step of: storing a third data portion using said first DMA channel.

22. The method of claim 21, further comprising the step of: reprogramming a register which contains said first address with a third address that is different than said first address prior to said step of storing said third data portion.

23. The method of claim 21, further comprising the step of: storing a fourth data portion using said second DMA channel.

24. The method of claim 23, further comprising the step of: reprogramming a register which contains said second address with a fourth address that is different than said second address prior to said step of storing said fourth data portion.

25. The system of claim 1, wherein each of said first and second sets of control registers further comprise at least one scratch register for storing status information which can be read by one of said master device and said slave device